Appendix K

Title:
Macro Specification
PMR Version 2.1

1 Introduction

1.1 Overview

The Protocol Machine Receive (PMR) provides protocol handling for a flexible number of logical channels. The PMR implements 4 modes, which can be programmed independently for each channel: HDLC, bit-synchronous PPP, octet-synchronous PPP and Transparent.

The configuration of each logical channel is programmed via the FPI slave bus and stored in the CSR - Context and Status RAM (or registers depending on the number of supported channels). The current state for the protocol processing (CRC check, channel state,...) is also stored in the CSR.

For the M256F, the performance requirements are 256 channels and a maximum serial rate of 43 Mbit/s. With an internal clock of 33 Mhz, 6 clock cycles are available in the average for loading of context, protocol handling of 8 bits and saving of context.

1.2 Features

- Protocol handling for a flexible number of logical channels
- Protocols supported: HDLC, bit-synchronous PPP, octet-synchronous PPP and Transparent mode
- Independent channel protocol configuration

1.3 System Integration

The PMR has four interfaces:

- FPI Slave Interface
- Timeslot Assigner (TSAR) Interface
- RB Interface
- Interrupt Bus

The PMR receives Timeslot data over the TSAR Interface and transmits the protocol data over the RB Interface. If during the Protocol handling a failure occurs (e.g., RB overflow or short frames) an interrupt vector is generated and written on the interrupt bus.

The PMR is configured (HDLC, PPP or Transparent mode) via the FPI slave bus.

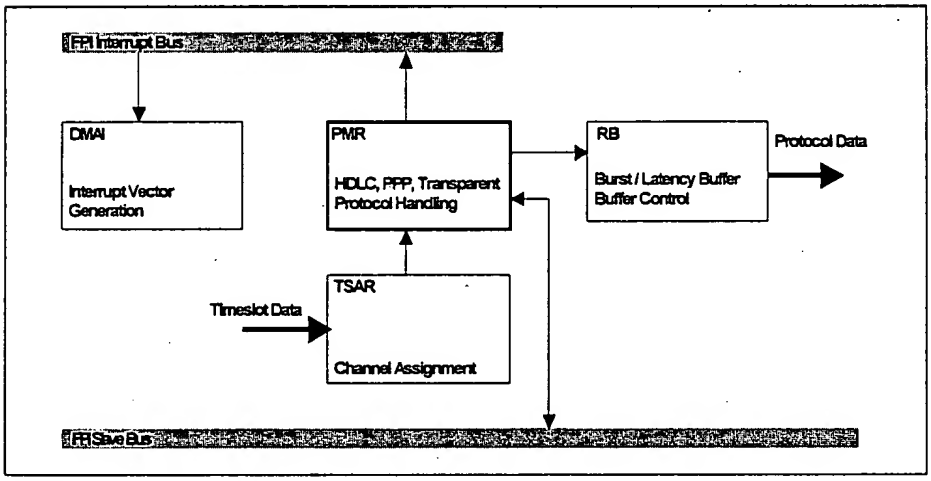


Figure 1
System Integration

1.4 Known Restrictions and Problems

2 Functional Description

2.1 Block Diagram incl. Clocking Regions

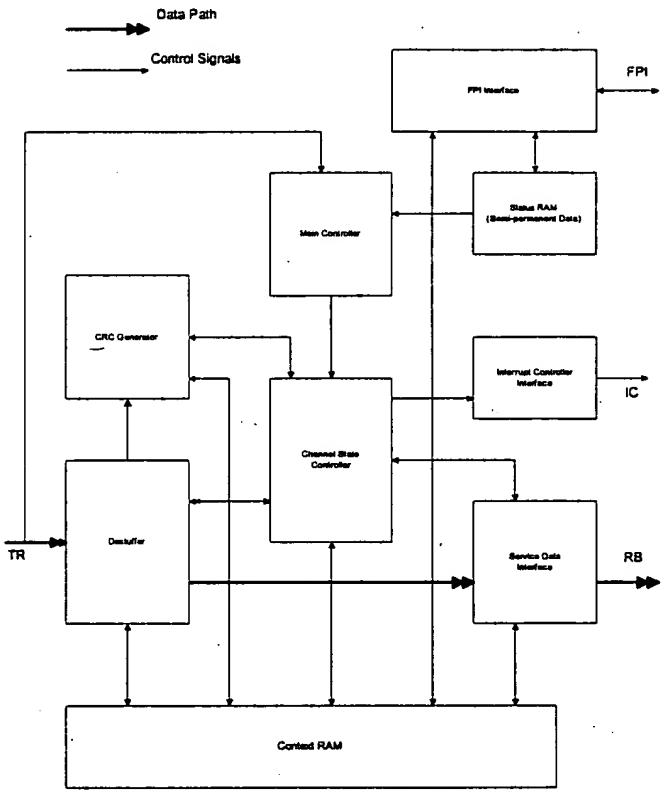


Figure 2
PMR Bock Diagram

2.2 Normal Operation Description

The TSAR will start a transfer to PMR by activating its TRWR_N line and providing the channel number (like the address bus on the FPI bus). In the second cycle TSAR will provide 8 bits data and the mask field (as bit enable lines). The PMR will load the context of the channel in the CSR, handle the 8 bits data and store the actual context again in CSR. Once 32 bits have been processed, PMR will transfer data to RB.

If subchannels are used (programming in the TSAR), the TSAR will still provide 8 bits data but will activate the TRMASK[7:0] lines. The masked bits are discarded and only the unmasked bits are handled by the protocol machine. In transparent mode, optionally, the masked bits can be replaced with '1' and then transferred to RB.

The CPU can turn off the reception of data for each channel via the command register. When a channel is turned off, a status with 'Frame End (FE)' and 'Receive Abort (RAB)' is transferred to RB (whether or not a frame is open) and the data received from TSAR is discarded until a channel initialization is performed again.

Interrupts are reported by generating interrupt vectors. If several interrupts occur in a very short period of time and could not be reported sequentially (e.g., the internal interrupt bus is busy), these interrupts (maximum of one for each interrupt type) are all stored in the context RAM and reported subsequently at the next possible time.

2.2.1 HDLC mode

Flag	Address	Control	Information	CRC	Flag
0111 1110	8 bits	8 bits	<=0 Bits	16/32 bits	0111 1110

Figure 3
HDLC Frame Format

The frame begin and end synchronization is performed with the flag character (7Eh). Shared opening and closing flag and shared 0 bit between two flags must be supported.

Prior to FCS computation, any '0' bit that directly follows five contiguous '1' bits is discarded. When closing flag is recognized, octet boundary check (bit number divisible by 8), CRC check, and short frame check is performed. The Maximum Frame Length (MFL) check is performed when a data octet is received. If CRC check is disabled, no short frame check is performed. Short frames are discarded in PMR (no transfer to RB). Only a SF interrupt vector is transferred to DMAI. If a CRC, MFL or octet boundary error is detected, data is transferred to RB with a status byte appended. The status byte is also generated when a frame end (closing flag) or an abort sequence (7 or more '1' are received) is detected. The following table describes the format of the word with status byte transferred to RB.

Table 1
Status word

Bit	31	30	29	28	27	26	25	24	23..	..16	15..	..8	7..	..0
Function	FE	MFL	RFO	CRC	ILEN	RAB	–	–	Byte3		Byte2		Byte1	

The number of valid bytes in the status word is indicated via separate signals to the RB.

RAB (Receive Abort), ILEN (Invalid Length), CRC (CRC error), RFO (Receive Frame Overflow), MFL (Maximum Frame Length), and FE (Frame End) bits are status bits transferred transparently through RB to DMAR.

Between two frames, the interframe time fill character can be either 7Eh or Idle pattern (15 contiguous 1's).

If no error, abort or frame end occurs, each time 32 bits are ready, they are transferred to RB. All the data between opening flag and closing flag with or without the CRC value (depending on the channel configuration register) is transferred.

Receive Overflow Error (RFO):

If the transfer to RB is not possible (no free entry in the buffer), RB will activate the RBFULL, and the PMR will then transfer a RFO interrupt (Receive Frame Overflow) to the DMAI and save RFO information in the channel context. The received protocol data (including flags, if any) will be silently discarded. When space is available in RB, the rest of the frame will be transferred and the status bit RFO will be set at the end of the frame, to indicate the software that the frame is not complete and experienced an RB overflow. The interrupt vector is an early warning for the CPU. A possible reaction to the RFO interrupt vector could be to slow down the transmission, so that more FPI and system bus band width is allocated to the receive path. Whenever an error-free frame is transferred to RB, the RFO interrupt, if stored in the context RAM is cleared.

Short Frame Error (SFE):

An SFL-CRC option is provided at the global level to define the lengths of short frame. If the SFL-CRC option is set to 0, then a frame is considered to be a short frame if less than 4 octets for CRC16 or less than 6 octets for CRC32 is received. If the SFL-CRC option is set to 1, then a frame is considered to be a short frame if less than 2 octets for CRC16 or less than 4 octets for CRC32 is received. If CRC check is disabled, then no short frame check is performed.

A flag followed immediately by an abort (01111110-01111111) is considered as a short frame of length 0 bytes. A flag followed by an abort with a shared 0 (01111110-1111111) is also considered as a short frame of length 0 bytes, provided these 7 1's do not form a

part of 15 contiguous 1's. Short frames of 0 length is reported even if CRC check is disabled.

Maximum Frame Length Error (MFL):

An MFL option along with the length of MFL (13-bits wide) can be specified. If the MFL option is not set, then the MFL length check is not performed. If the MFL option is set, the frame is considered invalid (MFL error) when the MFL+1st byte is received. This is independent of the CRC mode that is selected. The last bytes of data received depending on the CRC mode is not transferred to RB.

Invalid Length error (ILEN):

Whenever a frame is received containing not an integral number of 8-bit byte data, this error is reported.

CRC Error:

The CRC is checked only if CRC mode is enabled. If CRC error occurs, this is reported via the status information to the RB.

Receive Abort Error (RAB):

When 7 contiguous 1's are received in the middle of a frame, the RAB error is reported via status word unless it is a short frame.

Interrupt: Interframe fill changes

Whenever the interframe fill changes from Flag to Idle Pattern or vice versa, this condition is reported via two interrupts, interframe fill changed to flags and interframe fill changed to Idle Pattern. These interrupts can be masked on a per channel basis. The interframe fill is considered to be Flags when 2 or more flags (with or without shared 0) is received. The interframe fill is considered to be 'Idle Pattern' if 15 contiguous 1's are received at any time (e.g., after a current frame is aborted or after a closing flag or after MFL error is detected). After reset, the interframe fill is initialized to 'Idle Pattern'.

Interrupt: RFO

The RFO interrupt is generated when RB becomes full while a frame is being received. This interrupt can be masked on a per channel basis.

Interrupt: Short Frame

The Short Frame Interrupt is generated when a short frame is received. This interrupt can be masked on a per channel basis.

The parameters programmed in the channel configuration for HDLC mode are the following:

- Channel On/Off: Channel can be turned on or off using this bit
- CRC mode: 16 bit CRC (1+x5+x12+x16) or 32 bit CRC mode (1 + x + x2 + x4 + x5 + x7 + x8 + x10 + x11 + x12 + x16 + x22 + x23 + x26 + x32).
- CRC check suppression: in this case no short frame check is performed and all the data between opening and closing flag is transferred. However, short frames of length 0 bytes will not be transferred to RB independent of this option.
- CRC Transfer: If CRC check is enabled, this option specifies whether or not CRC is transferred to RB.
- Interrupt masks: This indicates whether or not the specific interrupt has to be masked.

Note: no address or control field recognition is performed

2.2.2 Bit synchronous PPP

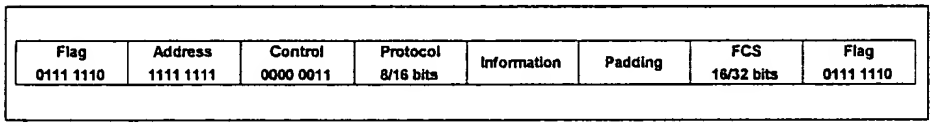


Figure 4
Bit synchronous PPP with HDLC framing structure

Same function in receive operation as in HDLC mode.The same parameters that apply to HDLC also apply to bit-synchronous PPP.

2.2.3 Octet Synchronous PPP

In the octet synchronous PPP mode, an octet stuffing procedure is used instead of the 0 bit insertion/deletion used for HDLC.

The frame begin and end synchronization is performed with the flag character (7Eh). Shared opening and closing flag must be supported but shared 0 bit between two flags is not allowed in this mode.

A table is maintained for each channel containing the Asynchronous Control Character Map (ACCM) for characters 00-1F $_{Hex}$. One programmable register is used to let the CPU select which of the 32 fixed characters are mapped using the Control Escape sequence. $7D_{Hex}$ and $7E_{Hex}$ in the data stream are always mapped.

On reception, prior to FCS computation, each octet with value less than hexadecimal 0x20 is checked in the ACCM. If it is flagged in the receiving ACCM, it is deleted. Each Control Escape octet is also removed, and the following octet is exclusive-or'd with hexadecimal 0x20, unless it is the Flag Sequence (which aborts the frame).

When closing flag is recognized, CRC check, and short frame check is performed. The Maximum Frame Length (MFL) check is performed when a data octet is received. If CRC check is disabled, no short frame check is performed. Short frames are discarded in PMR (no transfer to RB). Only a SF interrupt vector is transferred to DMAI. If a CRC or MFL error occurred, data is transferred to RB with a status byte appended. The status byte is also generated when a frame end (closing flag) or an abort sequence (escape, flag) is detected. Refer to **Table 1** for the format of the word with status byte transferred to RB. Note that an octet boundary check is not performed, because after the opening flag has been detected, the incoming data is handled at the octet level.

Between two frames, the interframe time fill character is always 7Eh.

If no error, abort or frame end occurs, each time 32 bits are ready, they are transferred to RB. All the data between opening flag and closing flag with or without the CRC value (depending on the channel configuration register) is transferred.

RFO Error:

If the transfer to RB is not possible (no free entry in the buffer), RB will activate the RB_FULL, PMR will transfer a RFO interrupt (Receive Frame Overflow) to the DMAI and save RFO in the context of this channel. The received protocol data will be silently discarded. When space is available in RB, the rest of the frame will be transferred and the status bit RFO will be set at the end of the frame, to indicate the software that the frame is not complete and experienced an RB overflow. The interrupt vector is an early warning for the CPU. A possible reaction to the RFO interrupt vector could be to slow down the transmission, so that more FPI and system bus band width is allocated to the receive path. Whenever an error-free frame is transferred to RB, the RFO interrupt, if stored in the context RAM is cleared.

Short Frame Error:

An SFL-CRC option is provided at the global level to define the lengths of short frame. If the SFL-CRC option is set to 0, then a frame is considered to be a short frame if less than 4 octets for CRC16 or less than 6 octets for CRC32 is received. If the SFL-CRC option is set to 1, then a frame is considered to be a short frame if less than 2 octets for CRC16 or less than 4 octets for CRC32 is received. If CRC check is disabled, then no short frame check is performed.

Maximum Frame Length Error:

An MFL option along with the length of MFL (16-bits wide) can be specified. If the MFL option is not set, then the MFL length check is not performed. If the MFL option is set, the frame is considered invalid (MFL error) when the MFL+1st byte is received. This is independent of the CRC mode that is selected. The last bytes of data received depending on the CRC mode is not transferred to RB.

CRC Error:

The CRC is checked only if CRC mode is enabled. If CRC error occurs, this is reported via the status information to the RB.

Receive Abort Error:

When a flag immediately following the control escape octet is received in the middle of a frame, the RAB error is reported via status word unless it is a short frame.

Interrupt: RFO

The RFO interrupt can be masked on a per channel basis.

Interrupt: Short Frame

The Short Frame Interrupt can be masked on a per channel basis.

The parameters programmed in the channel configuration for octet synchronous PPP mode are the following:

- All parameters mentioned for HDLC mode above are applicable.
- An ACCM map of 32-bits per channel specifying what characters in the range 0 to 1F (hex) are mapped.
- An extended ACCM map of 4 characters is maintained at a global level. For each channel, any or all of these 4 characters can be specified to be treated as ACCM character.
- For each channel, an indicator specifying whether or not DEL character should be treated as ACCM character.

2.2.4 Transparent mode

When programmed in transparent mode, the PMR performs fully transparent data reception without HDLC framing, i.e. without

- Flag insertion and deletion
- CRC generation and checking
- bit stuffing.

A programmable character (TFLAG) can be extracted if programmed with FA=1 in the channel specification register. For FA = 0 nothing is extracted.

A programmable sub-channel mode is supported. If subchanneling is not specified (logical channels of less than 64 kbit/s), the TSA_MASK[7:0] lines acts like bit enable lines. The masked bits (TSA_MASK line is low) are replaced with '1' by PMR and transferred together with the unmasked bits to RB after 4 octets have been received from TSAR. In this case FA must be set to '0' for this channel. If subchanneling is specified, only unmasked bits are used to derive the data bits.

To support superchannels (fractional T1 or T1) in the transparent mode, the start of the reception of data is synchronized to the start of a PCM frame (at the framer interface).

Therefore after initialization in transparent mode, the PMR will first stay in an initial state, where all the data received from TSAR are discarded until the TSAR_SYNC line is activated for the first time. The TSAR is responsible to activate the TSAR_SYNC line in the first DS0 timeslot associated to a logical channel composed of more DS0 timeslots.

If the RB is full the received data cannot be transferred. In this case, a status word with status of RFO is sent to RB and a new frame is started only after the next TSAR_SYNC is received.

Interrupt: RFO

The RFO interrupt can be masked on a per channel basis.

The parameters programmed in the channel configuration for transparent mode are the following:

- The extraction of a character with FA bit.
- The character to be extracted in receive operation (TFLAG).
- Subchannel mode: If subchannel is specified, only unmasked bits are used to derive the data bits. Otherwise, the masked bits are replaced with a '1' and handled as if 8-bits of data is received.

2.3 Context and Status RAM / Register (CSR)

The following table describes the context the PMR needs to load and store every time it gets data from TSAR.

Bit / Field Name	Number of Bits	Description
		SEMI-PERMANENT DATA
CH STATUS	1	Channel On/Off state
MODE	2	Protocol Mode (HDLC, Bit PPP, Octet PPP, Transparent Mode)
DISABLE CRC / TFF	1	HDLC/PPP Mode : Disable CRC check Transparent Mode: Transparent Flag Filter
CRC32 MODE / TMP	1	HDLC/PPP Mode : 0=CRC16, 1=CRC32 mode Transparent Mode: Transparent Mode Pack
CRC XFER	1	CRC transfer to RB
INVERT DATA	1	Invert Input Data before processing
E-ACCM	4	Extension ACCM Map in Octet PPP mode
DEL	1	Map the DEL character in Octet PPP mode
INT QUEUE ID	3	Channel Interrupt Queue Identifier
INT MASK - IFF	1	Mask for 'Interframe fill change' Interrupt
INT MASK - SFR	1	Mask for 'Short Frame' Interrupt
INT MASK - RFO	1	Mask for 'Receive Overflow' interrupt
ACCM / TFLAG	32 / 8	Octet PPP Mode: ACCM Map Transparent Mode: Transparent Flag Character
		TRANSIENT DATA
CH STATE	2	Channel State
IFF Indicator	1	Interframe fill last received (Flag or Idle pattern)
RFO	1	RB was full. Status bit appended and transferred to RB when space again available.
SAV ABORT	1	Abort received but not yet processed
FLAG COUNT	1	Number of flags received

Bit / Field Name	Number of Bits	Description
PENDING INT	4	The interrupts yet to be reported (waiting for Interrupt controller)
CRC	32	Current computed CRC
ONE_COUNT	4	Number of '1' for flag, 0 bit deletion, abort
REM BIT CNT	3	Remainder bit count
REM BITS	7	Remainder bits
NOSYNC	1	Channel in Nosync state (waiting for flag)
FLAG RECD	1	Last Flag Received
BYTE_COUNT	16	Byte count for maximum length check. If exceeded, MFL error bit set.
DATA BUF	56	Current data history (32 in case of CRC32 not transferred plus last 24 bits received)
DATA BUF CNT	3	Number of bytes in DATA BUF

2.4 Interrupt Vector

Following **Table 2** describes the interrupt vector format generated by the PMR.

Table 2
Interrupt Vector Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1	Int Type		0		Queue ID										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFO	SF	IF-FL	IF-ID					Channel Number							

Channel number

Identifies the channel where the interrupt occurred.

RFO

Indicates a Receive Frame overflow. The Protocol handler was unable to transfer data to the RB. As soon RB can store data again, a RFO status is appended to the frame.

SF

Indicates that a short frame is detected and discarded by the protocol handler.

IF-FL

Interframe fill changed to Flags. This means that atleast two flags with or without a shared 0 is received as interframe fill.

IF-ID

Interframe fill changed to Idle Pattern. This means that 15 contiguous 1's were received.

Queue ID:

Identifies the queue ID (channel specific).

Int Type:

Type of interrupt is set to 'channel interrupt', since only channel interrupts are generated by PMR.

2.5 Reset Behavior

The PMR can be reset by external HW reset pin or/and by a SW controlled reset.

All internal registers and functions are initialized to known states (RESET state).

After reset the reception of data is turned off for all the channels and all registers are accessible via the FPI slave bus for initialization.

2.6 Functional Test Description

2.7 Production Test Description

3 Macro Interfaces and Signal Description

All signals are active high until otherwise specified. Active low signals are designated by "_N" appended to their names. To make the design as re-usable as possible, a bus signal whose width is application dependent is specified with one of the following parameters:

Parameter name	Bus Type	Typical Value (bits)
		M256F
CN	Channel Number Bus	8
DB	Data/Status Bus	32
OC	Octet Count in Status Word Bus	2

3.1 Signal Description

In the following sections, "Flexible Peripheral Interconnect (FPI) Bus compliant" means that the specified bus uses a subset of the FPI features and satisfies the basic address and data cycle. Not all FPI signals are implemented because default values are sufficient for the application i.e. they can be coded as constants in the hardware. Refer to the FPI bus specification for details of the complete bus.

The following tables lists the FPI-Bus signals and additional out-band signals:

- PRSTAT to indicate if transferred word is status instead of pure data. Captured by RB during address phase.
- PRSTAT_OC to indicate the number of data octets (0 to 3) included in the status word.
- RBFULL to stop PMR transfers when the RB has no free buffer space.

Table 3
Macro Interfaces and Signal Description

Symbol name	I/O	Function
Clock and Reset		
SYSCLK	I	Internal clock (33 MHz) derived from FPI master bus
HW_RESET_N	I	General reset of DMAR. All registers and RAM reset
SW_RESET_N	I	General reset of DMAR. All registers and RAM reset
STOP	I	Stop mode (or test mode).
PR_IIP	O	PR initialization in progress following reset. PR is not availble when this signal is asserted. This signal will remain high for several clocks following release of PR reset(s).
Timeslot Assigner (TSAR) Interface		
TRD[7:0]	I	8 bit data from Time Slot Assigner
TRCH[CNB-1:0]	I	Logical Channel Number (address bus cycle).
TRMASK[7:0]	I	8 bit Mask field to enable single bits of TRD
TRWR_N	I	Request for writing data. Transfer if active.
TRSYNC	I	Logical Channel Synchronization line
PR_TRRDY	O	Protocol data accepted
Receive Buffer (RB) interface		
PR_RBWR_N	O	Only single word write transfer is supported. Transfer if active, no operation otherwise.
PR_RBA[CNB-1:0]	O	Address of bus cycle corresponding to channel number
PR_RBD[DBB-1:0]	O	Output data to be written in the RB
RBRDY	I	Acknowledge signal when PR_RBD is written in RB
PR_RBSTAT	O	Active if Status byte is transmitted in the data word on PR_RBD

Table 3
Macro Interfaces and Signal Description (cont'd)

Symbol name	I/O	Function
PR_RBSTAT_OC [OC-1:0]	O	The number of octets (0 to 3) included in the status word
RBFULL	I	Asserted at end of PMR write cycle if: • Buffer free pool becomes empty or • FIFO task buffer to the DMA channel becomes full. De-asserted after DMAR read cycle.

Interrupt Controller (DMAI) Interface

PR_ICREQ_N	O	Master Request Line
ICGNT_N	I	Master Grant Line
PR_ICD[31:0]	O	Data Bus

FPI Slave Interface

TFPI_A[3:0]	I	Address bus.
PB_TFPI_D[DB-1:0]	I	Data bus. Active during data phase.
TFPI_D[DB-1:0]	I	Daisy Chain data bus input
PR_TFPI_D[DB-1:0]	O	Data bus. Active during data phase.
TFPI_WR_N TFPI_RD_N	I I	Read/Write controls. Following codes are defined: WR_N = 1; RD_N = 1 => NOP WR_N = 0; RD_N = 1 => data written to PMR WR_N = 1; RD_N = 0 => data read from PMR
TFPI_VG_SEL_N	I	Virtual Global Select. Global data for PMR (e.g., MFL) is updated using this select signal.
TFPI_VC_SEL_N	I	Virtual Channel Select. Channel specific data (e.g., disable CRC) is updated using this select signal.
TFPI_PR_SEL_N	I	PMR Select. PMR macro specific data is updated using this select signal.
PB_TFPI_RDY	I	Ready enable. The select signal from TFPI is processed only when this signal is active.
PR_TFPI_RDY	O	PMR action completed

3.2 Data Flow and Functional Timing

3.2.1 FPI Slave Bus

Refer to the SIEMENS FPI Bus for Munich-Macros Specification.

3.2.2 Timeslot Assigner (TSAR) Interface

The transfer is started by TSAR with the TRWR_N line. In the same cycle the channel number is activated. In the next cycle, the data and mask line is transferred.

For the first active timeslot of each logical channel, the TSAR activates the TRSYNC line.

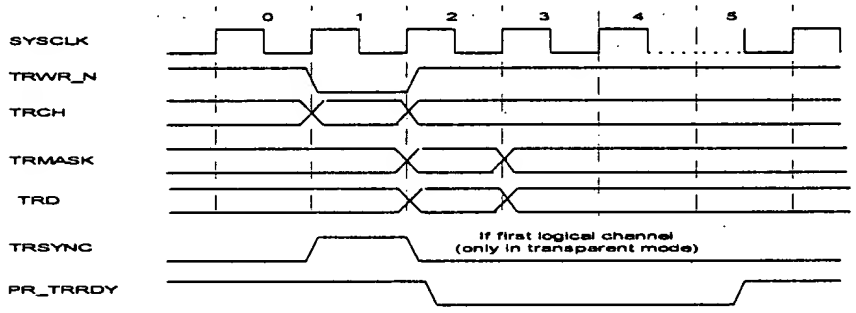


Figure 5
Data transfer from TSAR to PMR

3.2.3 RB Interface

The RB interface to the PMR is based on a unidirectional FPI slave bus. Only two operation codes, NOP and Single Word Transfer, are defined. The write signal WR_N is used to indicate a single word tranfer to RB from PMR. The select signal SEL_N is implicitly active and not physically present. The PMR initiates an address cycle by asserting the WR_N. RB captures the channel number from the address bus during this cycle. During the data cycle, RB captures the data as soon as possible. RB asserts RBRDY during the clock cycle that it can complete the data transfer.

Following out-of-band signals are required

1.PMR_STAT to indicate if transferred word is status instead of pure data. Captured by RB during address phase.

2.PRSTAT_OC to indicate the number of data octets (0 to 3) included in the status word

3.RBFULL to stop PMR transfers when the RB has no free buffer space.

The PMR bus does not support overlapped transfers. The RBFULL signal is asserted simultaneously with RBRDY. PMR must not attempt another transfer until this flag is de-asserted.

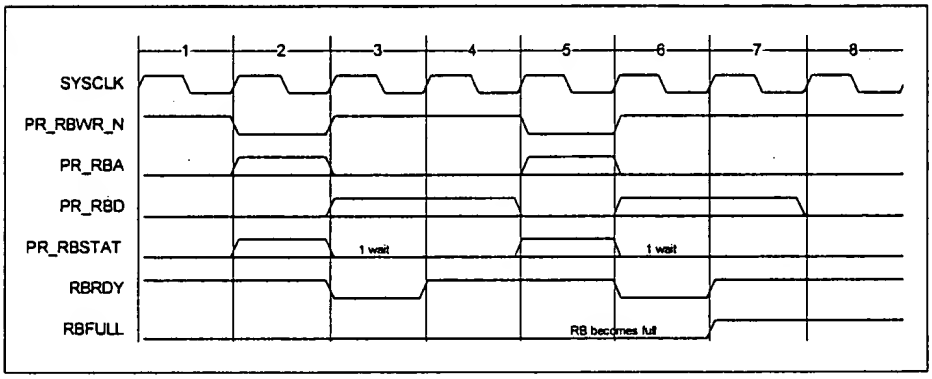


Figure 6
Two word transfer from PMR to RB

3.2.4 DMAI Interface

The interrupt vector is transferred to the DMUI on the interrupt bus. PMR asserts the PR_ICREQ_N and waits for the ICGNT_N grant. When the grant is received, PMR removes the request at the beginning of the next clock cycle and asserts the PMR interrupt vector. No other handshaking is required.

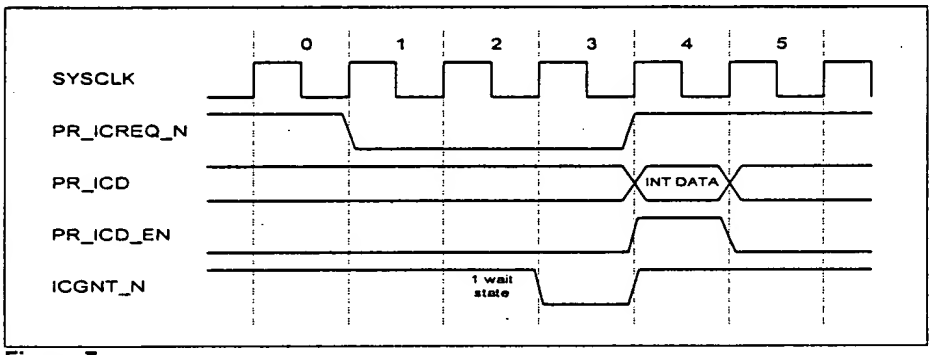


Figure 7
Two Interrupt transfers to DMAI

3.3 Macro Functional Test

3.4 Macro Production Test

4 Register Description

4.1 Register Overview

The PMR specific registers allows initialization and turn off of the protocol handler for each channel.

4.2 Detailed Register Description

4.2.1 Configuration Register 1 (CONF1)

Access : read/write

Offset Address : 00_H

Reset Value : 83000060_H

31GC GC GC

IIP (read only)	0	0	0	0	0	STOP	SW_RESET	0	0	MFLE	MFL(12:8)

15

MFL(7:0)	MBIM	PBIM	RBIM	0	SFLCRC	RBM	LBE	GPM

Note: This register is implemented once in the chip !

GPM: General PCM Port Mode:
'0' : Standard Channelized Mode;
'1': Alternate Channelized Mode: 8 * T1/E1 lines (port 0...7) without chip internal framing function

LBE: Little/Big Endian Byte Swap: '0': Little Endian ; '1' : Big Endian

RBM: Receive Buffer Monitor: if set to '0', the minimum free pool count is captured in register RBTH; if set to '1' an interrupt is generated, if the free pool counter falls blow the value programmed in register RBTH

SFLCRC: '0': short frame is detected, if a received frame contains < 4 bytes (CRC16)

or < 6 bytes (CRC32)
'1': short frame is detected, if a received frame contains < 2 bytes (CRC16) or < 4bytes (CRC32)

RBIM: Receive Buffer Interrupt Mask: if set to '1' the receive buffer threshold system interrupts (RAEW,RBEW) are not generated

PBIM: PCI Interface Interrupt Mask: if set to '1' the PCI Interface interrupt is not generated.

MBIM: Mailbox Interrupt Mask: if set to '1' the Mailbox interrupt to the PCI interface is not generated

MFL(12:0): Maximum Frame Length check against this value is performed, if MFLE ='1'

MFLE: The maximum frame length check is enabled (='1') or disabled (='0')

SW_RESET: if set to '1', the software reset is activated; software reset has generally the same effect on the HDLC part as hardware reset with two exceptions:
- outputs are not tristated
- the bit SW_RESET itself is not reset; it has to be deactivated by software again

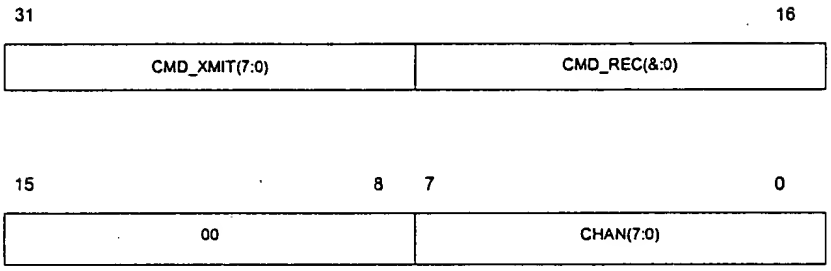
STOP: '1' means : device is in "Fast Software Initialisation Mode" (for customers only applicable after reset!); '0' : device is in normal operation

IIP: Initialization in Progress (Read Only): If '1', internal RAMs are being self initialized by the device; no other access than to this register is possible

Note: Only the following fields are handled by PMR:
SFLCRC,
MFL
MFLE

4.2.2 (Virtual) Channel Specification Command (CSPEC_CMD)

Access : write
Address : 20_H
Reset Value : 00000000_H



Note: The Virtual Channel Spec (VCS) Command Register has to be programmed after all other required VCS registers, in order to initiate the programming of all macros. In case of a debug command, first the command register has to be written, then a broadcast read of the virtual channelspec is possible by read of all VCS data registers. Only the macro which has implemented the corresponding bit has to drive the register bit, otherwise drives '0' to provide broadcast read feature.

Note: ONLY THE RECEIVE COMMANDS ARE HANDLED BY PMR.

CHAN(7:0): selected channel number to be programmed

CMD_REC(7:0): for details refer to table "Command Description"

Commands Receive:

1. Receive Init
2. Receive Abort
3. Receive Off
4. Receive Hold Reset
5. Receive Debug
6. Receive NOP

CMD_XMIT(7:0): for details refer to table "Command Description"

Commands Transmit:

1. Transmit Init (sets up a TBUFFER= ITBS automatically)
2. Transmit Abort
3. Transmit Off; (shuts down the TBUFFER to NITBS=0 automatically (regardless of NITBS register contents)
4. Transmit Hold Reset
5. Transmit Debug
6. Transmit NOP (no operation)
7. Transmit Idle (Sends IDLE code as programmed in CONF3 on the channel)

Note: Transmit Init for a channel must be programmed only after reset or after a Transmit Off command, i.e. two Transmit Init commands for the same channel are not allowed

Command Table Receive:

23	22	21	20	19	18	17	16	
Rsvd	Rsvd	Rsvd	Debug	HOLD RESET	ABORT	OFF	INIT	function
0	0	0	0	0	0	0	1	receive init
0	0	0	0	0	0	1	0	receive off
0	0	0	0	0	1	0	0	receive abort
0	0	0	0	1	0	0	0	receive hold reset
0	0	0	1	0	0	0	0	receive debug
0	0	0	0	0	0	0	0	receive nop

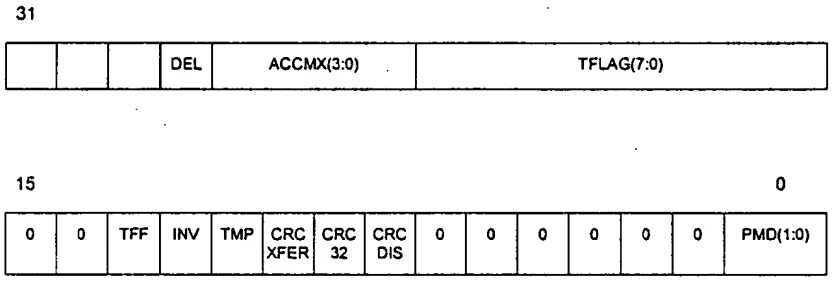
Command Table Transmit:

31	30	29	28	27	26	25	24	
Rsvd	Rsvd	Rsvd	Debug	HOLD RESET	ABORT	OFF	INIT	function
0	0	1	0	0	0	0	0	transmit idle
0	0	0	0	0	0	0	1	transmit init

31	30	29	28	27	26	25	24	
0	0	0	0	0	0	1	0	transmit off
0	0	0	0	0	1	0	0	transmit abort
0	0	0	0	1	0	0	0	transmit hold reset
0	0	0	1	0	0	0	0	transmit debug
0	0	0	0	0	0	0	0	transmit nop

4.2.3 (Virtual) Channel Specification Mode Receive (CSPEC_MODE_REC)

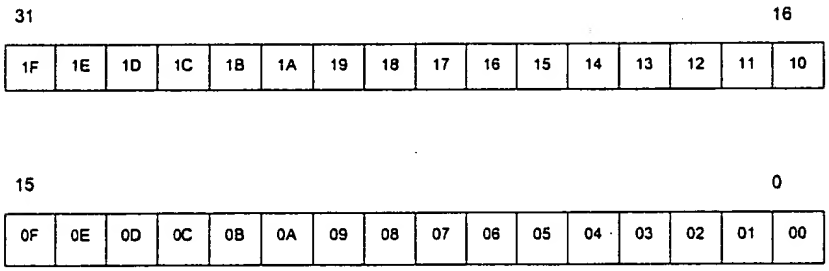
Access : read/write
Address : 24_H
Reset Value : 00000000_H



PMD(1:0): Protocol Machine Mode
CRCDIS: '0': CRC check is enabled; '1': CRC check is disabled
CRC32: if set to '1', add CRC32 checksum; otherwise add CRC16 checksum
CRCXFER: '0': CRC is not transfered to the shared memory; '1' CRC is transferred to the shared memory; if CRCXFER is selected the short frame check is not applied to the received data
TMP: Transparent Mode Pack: '1': if subchanneling is used in transparent mode (i.e. less than 8 bits of a time slot are used), the non-used (masked) data bits are discarded;
'0': the non-used (masked) data bits are substituted by '1's
INV: '1' all received data in this channel are inverted; '1': no inversion
TFF: function identical to FA in transmit direction (only transparent mode)
TFLAG(7:0): used only in transparent mode; these bits constitute the flag that is filtered from the received bit stream
ACCMX(3:0): Extended ACCM: a '1' enables the corresponding character in CSPEC_REC_ACCMX
DEL: Del Map flag

4.2.4 (Virtual) Channel Specification Receive ACCM Map (CSPEC_REC_ACCM)

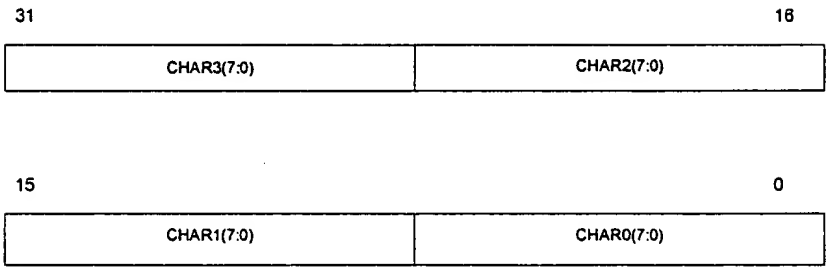
Access : read/write
Address : 28_H
Reset Value : 00000000_H



This map is used by a channel in octet synchronous PPP mode only. If a bit is set, the corresponding character is expected to be mapped by the Control ESC character and is hence ignored, if received.

4.2.5 Receive Extended ACCM Map (REC_ACCMX)

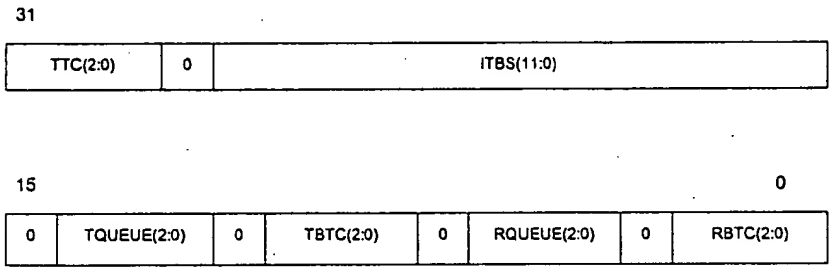
Access : read/write
Address : $2C_H$
Reset Value : 00000000_H



This register is only used by a channel in octet synchronous PPP mode. A character written to this register will be mapped with a Control Escape sequence, if the corresponding enable flag is set in the CSPEC_MODE_REC register (ACCMX(3:0)).

4.2.6 (Virtual) Channel Specification Buffer (CSPEC_BUFFER)

Access : read/write
Address : $3C_H$
Reset Value : 00000000_H

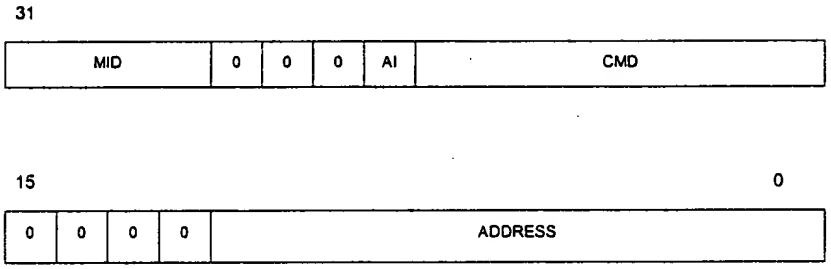


RBTC: receive burst threshold code (affects RB)
RQUEUE: The generated receive interrupts will be sent to this interrupt queue
TBTC: transmit burst threshold code (affects TB)
TQUEUE: The generated transmit interrupts will be sent to this interrupt queue
ITBS: individual transmit buffer size (affects TB);
TTC: Transmit Threshold Code

Note: Only the Receive Interrupt Queue (RQUEUE) is processed by PMR.

4.2.7 Test Command Register (TAC)

Access : write
Offset Address : FE_H
Reset Value : 00000000_H



MID: Macro ID Code
AI: Auto Increment Function
Address: internal address
CMD: Command (select of ram and register)

CMD:

23	22	21	20	19	18	17	16	
								function
0	0	0	0	0	0	0	0	tbd (macro spec)

Macro ID Code:

31	30	29	28	macro
0	0	0	0	PMR
0	0	0	1	PMT
0	0	1	0	RB

31	30	29	28	macro
0	0	1	1	TB
0	1	0	0	DMUR
0	1	0	1	DMUT
0	1	1	0	TSAR
0	1	1	1	TSAT
1	0	0	0	XPI
1	0	0	1	DMUI

General

- the test access provides read/write access of important internal rams and registers
- test registers are virtuals global registers (SEL signal: pb_vg_tfpi_sel_n / implemented as a daisy chain).
- the single macros are selected by the MID code of the test command register
- the test access provides read/write access of important internal rams and registers
- CMD specifies/selects one of the macro rams/registers
- the address field is used to access a ram address
- AI: autoincrement : address given in the address field is incremented automatically for each access
- All macros which are not selected by MID drive data output "00000000" and <macro>_TPFI_RDY = '1'. Driving "00000000" would mean not disable the enable line for data out, but to set the output data to "00000000".

Test write access:

1. Write TAC
2. Write TAD

Test read access:

1. Write TAC
2. Read TAD

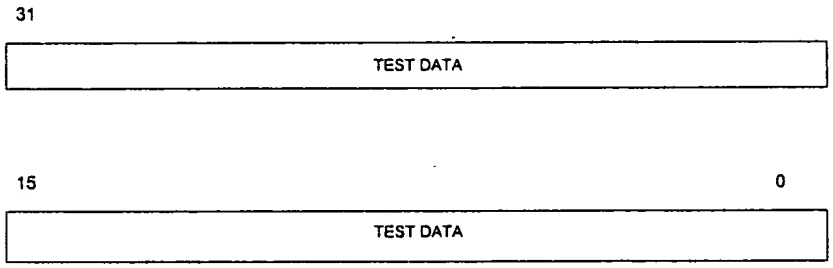
Typically the macro selected via MID delays the RDY signal until the selected ram/ register has been read and the data can be provided at the TFPI interface. No prefetch of testdata is required.

CMD:

0: Configuration RAM 0- all data excluding ACCM
1: Configuration RAM 1- ACCM
2: Transient RAM 2- CRC
3: Transient RAM 3- data buffer word (first 4 bytes of data buffer)
4: Transient RAM 4- data buffer remaining 3 bytes, data buffer count
5: Transient RAM 5 - destuffer context, Frame Length
6: Transient RAM 6 - channel state context, save abort, interrupts, interframe fill state, flag count
7: Stop PMR
8: Continue PMR

4.2.8 Test Data Register (TD)

Access	: read/write
Address	: FF_H
Reset Value	: 00000000_H

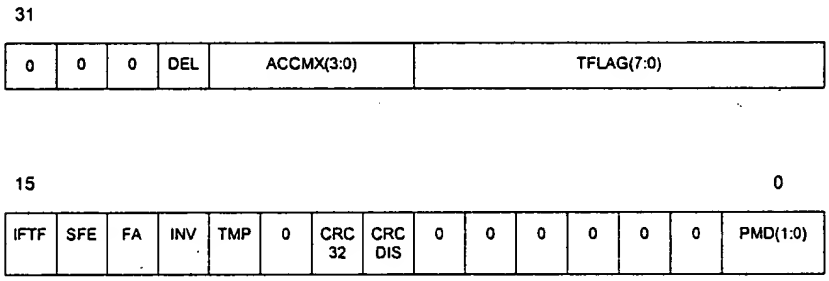


TEST DATA: ram/register test data (read or write)

Note: It is assumed that a TFPI_SEL_N signal is generated for register access of common TAC and TD register. For write / read access the MID (macro ID) is used for addressing one macro: If MID does not match with the hard coded ID, TFPI_D are prepared corresponding the 'daisy chain' requirements.I.e. each macro drives "00000000". These '0' s are ored in the macroshell.

4.2.9 (Virtual) Channel Specification Mode Transmit (CSPEC_MODE_XMIT)

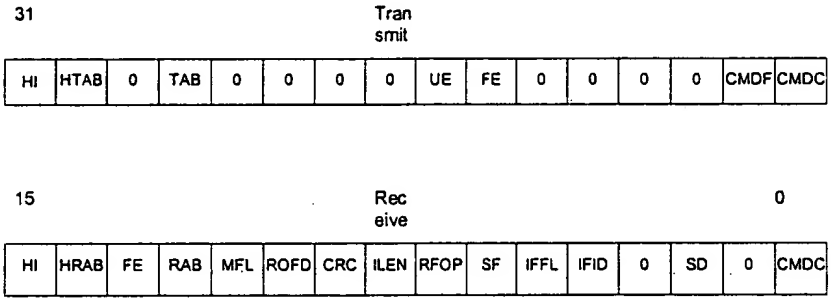
Access : read/write
Address : 30_H
Reset Value : 00000000_H



PMD(1:0): Protocol Machine Mode
CRCDIS: '0': CRC is transmitted; '1': CRC is not transmitted
CRC32: if set to '1', add CRC32 checksum; otherwise add CRC16 checksum
TMP: Transparent Mode Pack: '1': if subchanneling is used in transparent mode, the adjustment of transmit data is done automatically;
'0': the non-used bits are expected to be '1's in the shared memory
INV: '1' all transmit data in this channel are inverted; '1': no inversion
FA: flag adjustment (only transparent mode) selected
SFE: Shared Flag Enable: '0' 2 flags are sent at least between (HDLC, PPP?) frames; '1' flag is sent at least between (HDLC,PPP?) frames
IFTF: Interframe Time Fill: '0': $7E_H$; '1': FF_H
TFLAG(7:0): used only in transparent mode; these bits constitute the flag that is inserted into the transmit bit stream
ACCMX(3:0): Extended ACCM:
DEL: Del Map flag

4.2.10 (Virtual) Channel Specification Interrupt Mask/Queue (CSPEC_IMASK)

Access : read/write
Address : 48_H
Reset Value : $FFFFFFFF_H$



Interrupt Generation Mask: These bits correspond to the respective channel interrupts, if set to '1', the corresponding interrupt will not be generated by the device

SD : Silent Discard Mask: If set to '1' the HRAB+RAB interrupt, which occurs, when receive frames are discarded during HOLD is masked

5 Functional Test Specification (Macrolevel)

(use Checklist C06 "Function Checklist - Comparison of Specification vs. Circuit"
http://www.hl.siemens.de/lognet/hl_ta/dhb/f.htm)